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ELECTRON TRAPPING MECHANISM IN A MULTI-LEVEL ORGANIC FET MEMORY USING LITHIUM-ION-ENCAPSULATED FULLERENE AS THE FLOATING GATE

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Abstract. We report on the electron trapping mechanism in a multi-level organic field effect transistor (OFET) memory using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as the floating gate. Based on the estimation of trapped electron number per each $Li^+@C_{60}$ molecule when a programming voltage was applied, the active domain of the floating gate was determined to be the surface of the $Li^+@C_{60}$ domain. An analysis of the cyclic voltammetry indicated that each $Li^+@C_{60}$ molecule can trap electrons at the trapping energy level of -4.94 and -4.49 eV. The number of trapped electron was confirmed by the ultraviolet-visible spectroscopy (UV-Vis).

Keywords: Organic field-effect transistor, Multi-level memory, Lithium-ion-encapsulated fullerene

1. INTRODUCTION

Memory based on organic field-effect transistor (OFET) has received considerable attention due to its advantages such as mechanical flexibility, low-cost, and suitability for large-area fabrication [1,2]. The memory OFET could be obtained by using a ferroelectric

material as the gate dielectric layer. By programming with an applied voltage to the gate, the polarization of the gate dielectric will induce charges in the channel of the transistor, which results in the increase of the drain current (I_D) of the OFET. After the programming voltage removal, the remnant polarization will keep the I_D high, which determines the programmed state from the initial state [3,4]. Ferroelectric memory OFET with its simple structure exhibited a high performance. However, the ferroelectric material of poly (vinylidene fluoride-co-trifluoroethylene) (P(VDF-TrFE)) polymers are semi-crystalline, which makes thin layer rough. In addition, the depolarization of ferroelectric gate layer will reduce the retention time of the memory. Another method to obtain the memory effect in the OFET is an employment of a polymer electret [5,6] or a floating gate [7] as the charge trapping layer. In this concept, by programming, charges are injected from the source/drain (S/D) electrodes and then trapped at the polymer/silicon dioxide (SiO_2) interface (in the polymer electret structure) or at the floating gate (in the floating gate structure). After the programming voltage removal, the trapped charges will induce the I_D in the OFET corresponding to the memory effect. Although the memory OFETs using polymer electret are reported in many papers [5,6], the understanding of the charge trapping mechanism is still limited. In the term of floating gate memory OFET, the charges are injected into the floating gate normally by hot-carrier injection or Fowler-Nordheim tunneling [8]. Then, injected charges are trapped in the floating gate of Al, in the gold-nanoparticles (Au-NPs), or around of the hybrid composite polymer/NPs of Au [7] and zinc oxide (ZnO) [9]. A variety of researches on floating gate memory OFETs indicates that this type of memory and its operation mechanism still have attracted much research interest.

Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$), which contains a Li cation inside a fullerene cage, has been researched recently [10,11]. The one-electron reduction potential of $Li^+@C_{60}$ is higher than that of pristine fullerene [10,11] indicated that this material is promising to accept electrons. Thus, it is high possible to use $Li^+@C_{60}$ as the floating gate in the memory OFETs. In addition, the multiple reduction/oxidation peaks of $Li^+@C_{60}$ suggests that the number of trapped electrons may be controlled by an applied voltage, which is the key point to fabricate a multi-level memory.

The fabrication of the multi-level memory OFETs was presented in our report. [12] These memory devices exhibited multi-level memory characteristics with the ΔV_{th} of 10, 16, 32 V after programming by an applied voltage of 150 V for 0.5, 5, and 50 seconds. The memory effect was concluded to be the trapped electron in the $Li^+@C_{60}$ layer. In this article, we analyze the electron trapping mechanism of the $Li^+@C_{60}$. By estimation the number of trapped electron per each $Li^+@C_{60}$ molecule, we conclude that only $Li^+@C_{60}$ molecules at the surface of the $Li^+@C_{60}$ domains are active, in which electrons are trapped. The cyclic voltammetry (CV) of the $Li^+@C_{60}$ salt was conducted to calculate the trapping site, where electrons are trapped at energy potential of -4.94 and -4.49 eV, respectively. In addition, the ultraviolet-visible spectroscopy (UV-Vis) spectra of $Li^+@C_{60}$ thin film showed 2 absorption peaks at wavelength of 470 and 700 nm, which was an evidence of the trapped electrons in the $Li^+@C_{60}$ molecules under an applied voltage.

2. EXPERIMENTAL

Figure 1 shows the structure of the memory OFET in this study. The fabrication process of the memory OFET could be found elsewhere in our previous report. [12] To estimate the number of trapped electron in $Li^+@C_{60}$ molecule, the density of trapped electron in the $Li^+@C_{60}$ layer (ΔN) was calculated based on the shift of the $V_{th.}$ On the other hand, the density of $Li^+@C_{60}$ molecules in floating gate (N_{Li}) was roughly estimated based on the density of $Li^+@C_{60}$ and its distribution in this layer.

To clarify the trapping site of electrons in the $Li^+@C_{60}$ molecules, a cyclic voltammetry (CV, Autolab PGSTAT302N by Metrohm) was carried out with a solution of $Li^+@C_{60}$ bis(trifluoromethylsulfonyl)imide ($Li^+@C_{60}$ NTf_2^-) in benzonitrile (PhCN) with a concentration of 10^{-4} M consists of an electrolyte of tetrabutylammonium hexafluorophostate ($TBAF_6$) (0.1 M). The CV measurement was conducted using the working electrode of platinum (Pt), the reference electrode of Ag/Ag^+ and the scan rate of 100 $mV{\cdot}s^{-1}$.

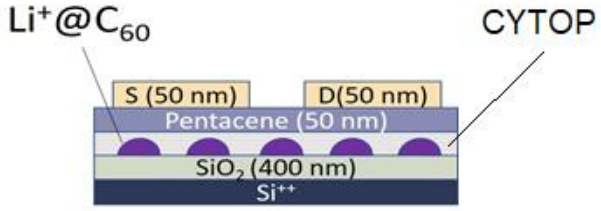

Fig. 1. *Schematic structure of the memory OFET.*

To confirm the electron trapping ability of $Li^+@C_{60}$, a capacitor was prepared for an absorption spectroscopy measurement (Jasco V-570 UV-Vis-NIR Spectrophotometer). On the glass substrate with indium tin oxide (ITO), an active layer of the capacitor was deposited by spin-coating at a speech of 2,500 rpm for 30 second using a solution of a mixture of $Li^+@C_{60}$ NTf_2^- and poly vinyl cinnamate (PVCN) (1:8) in mono chlorobenzene with a concentration of 45 mg/ml. Subsequently, the substrate was subjected into ultraviolet exposure for 20 min for photo-crosslinking, followed by dried at 140ºC for 1 h. Finally, an aluminum (Al) electrode was fabricated by thermal deposition. The thickness of the Al electrode was 100 nm. Another capacitor with an active layer of PVCN was prepared under the same fabrication process for comparison.

The fabrication and the measurement processes were carried out completely in the cleaning room at Japan Advanced Institute of Science and Technology (JAIST).

3. RESULT AND DISCUSSION

3.1. Electron trapping at $Li^+@C_{60}$ molecule under applied voltage

The memory characteristics of the memory OFET which was shown in Fig.1 were presented in our previous report [12]. Under a programming voltage of 150 V for 0.5, 5, and 50 seconds, the transfer curve shift to the positive gate voltage (V_G) region, causing the memory window (ΔV_{th}) of 10, 16, and 32 V, respectively. For erasing the data, a reversed

voltage of -150 V was used for 0.17, 1.7, and 17 seconds. The memory OFET behaved as a multi-level memory, which was reported in literature [13]. The origin of the memory effect was supposed to be the trapped electron in the $Li^+@C_{60}$ layer. The ΔN was calculated using the equation [14].

$$\Delta N = \frac{\varepsilon \cdot \Delta V_{th}}{d \cdot e} \quad (1)$$

where ε, d are the permittivity (1.86×10^{-13} F·cm^{-1}) [15] and the thickness of the insulator Cytop, e is the elementary charge and ΔV_{th} is the shift of the V_{th}. Follow our previous report, the ΔN was increased with the duration of programming voltage [12].

The density of the floating gate (N_{Li}) can be estimated from the its distribution on the SiO_2 surface and the molecular density of $Li^+@C_{60}$ salt if this layer was stable after the insulator fabrication. Figure 2(a) and 2(b) show the morphology of $Li^+@C_{60}$ on the SiO_2 surface before and after spin-coating the insulator of Cytop (AFM, Hitachi SPA 400). As shown in the Fig. 2a, the $Li^+@C_{60}$ layer was formed as domains on the SiO_2 surface. These domains are still observed after the insulator fabrication (Fig. 2(b)). It indicated that the $Li^+@C_{60}$ are stable and would act as the floating gate in the memory device. Since the $Li^+@C_{60}$ domains distributed as islands on the SiO_2 surface, we assumed that the average roughness (S_a) of this surface is refer to the thickness of the floating gate. The S_a was estimated to be 8.00 nm. S. Aoyagi *et al*. reported a cubic of $Li^+@C_{60}$ hexa-chloroantimonate ($Li^+@C_{60}$ $SbCl_6^-$) contained 4 molecules had a volume of 3,554.6 Å^3. [16]. We assumed that the crystal structure of $Li^+@C_{60}$ NTf_2^- was similar with those of $Li^+@C_{60}$ $SbCl_6^-$. Thus, the molecular density of $Li^+@C_{60}$ NTf_2^- was estimated to be 1.88 g·mol^{-1}. Based on these results, the N_{Li} was roughly estimated to be 9.00×10^{14} cm^{-2}.

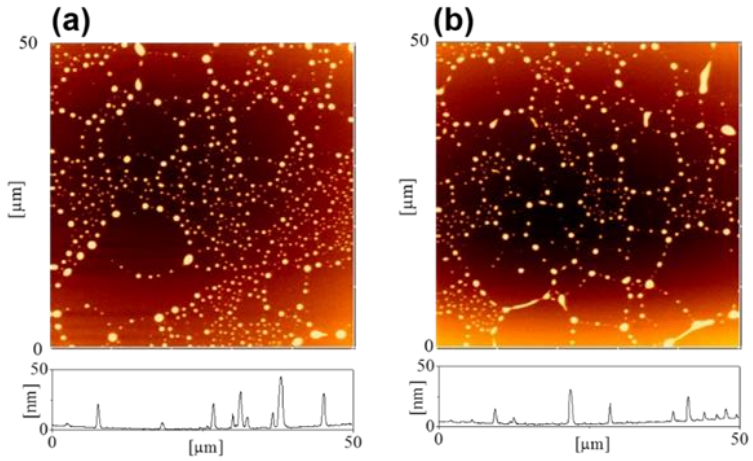

Fig. 2. *Morphology with a cross section profile of $Li^+@C_{60}$ layer on the SiO_2 surface (a) before and (b) after spin-coating a layer of Cytop.*

Under the programming voltage of 150 V for 0.5, 5 and 50 s, count per area unit, ΔN electrons would be injected into N_{Li} $Li^+@C_{60}$ molecules of the floating gate. If all $Li^+@C_{60}$ molecules had trapped electrons, the average number of trapped electron per $Li^+@C_{60}$ molecule would have been 2.40×10^{-2}, 3.84×10^{-2}, and 7.68×10^{-2} electrons, respectively. It indicated that electrons would not be trapped by all $Li^+@C_{60}$ molecules. We proposed that only the $Li^+@C_{60}$ molecules at the surface of the floating gate were active and trapped the

electrons.

3.2. Trapping site of electron in $Li^+@C_{60}$

To investigate the possible number of trapped electrons into a $Li^+@C_{60}$ molecule, the CV measurement was carried out. Figure 3 shows the CV of $Li^+@C_{60}$ NTf_2^- (10^{-4} M) in the solution of PhCN containing the electrolyte of $TBAPF_6$ (0.1 M). The first onset electron reduction potential of $Li^+@C_{60}$ NTf_2^- was found to be 0.23 V and the second one was -0.22 V. It means that each $Li^+@C_{60}$ molecule can trap up to 2 electrons. From the Fig. 3, the trapped electrons can occupy at the LUMO level of -4.94 and -4.49 eV using the equation [17]

$$LUMO = -e\left[E_{onset(red)} + 4.71\right] \quad (2)$$

where $E_{onset(red)}$ is the onset reduction potential, which is obtained from the reduction peak vs the reference electrodes of Ag/Ag^+.

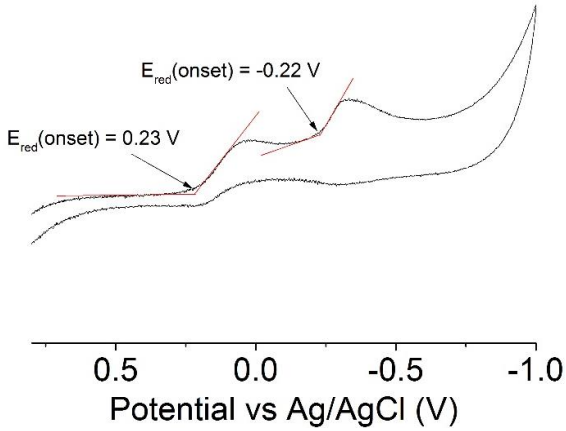

Fig. 3. *CV of $Li^+@C_{60}$ NTf_2^- (10^{-4} M) recorded in PhCN containing 0.1 M $TBAPF_6$.*

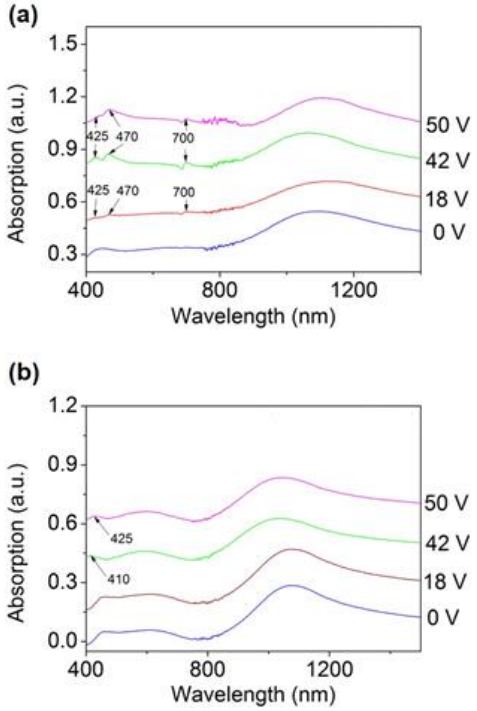

Fig. 4. *UV-Vis spectra of PVCN capacitor (a) with and (b) without $Li^+@C_{60}$ NTf_2^- after applying the bias voltage.*

To confirm the possible number of trapped electron per $Li^+@C_{60}$ molecule, the UV-Vis measurement was conducted. Figure 4(a) and 4(b) show the normalized UV-Vis spectra of the capacitor with an active layer of PVCN containing and without $Li^+@C_{60}$ NTf_2^-. As shown in Fig. 4(a), the unstable signal at the wavelength between 760 and 900 nm could be the noise during measurement, which caused by the measurement system. The shift of a tumor at the wavelength between 1,000 and 1,200 nm could be due to an interference effect. Under the bias voltage of 18, 42, and 50 V, we found the increase of peaks at the wavelength of 425, 470 and 700 nm. On the other hand, the UV-Vis spectra of the sample without $Li^+@C_{60}$ NTf_2^- only showed the existence of the peak at the wavelength of 425 nm. It clearly indicated that the peak at the wavelength of 470 and 700 nm corresponds to the trapped electrons into $Li^+@C_{60}$ molecules under the applied voltage. Based on this result, we conclude that each $Li^+@C_{60}$ molecule could trap 2 electrons by applied voltage. These 2 electrons can receive photon energies and move to an excited state which corresponds to the absorption peaks at the wavelength of 470 and 700 nm.

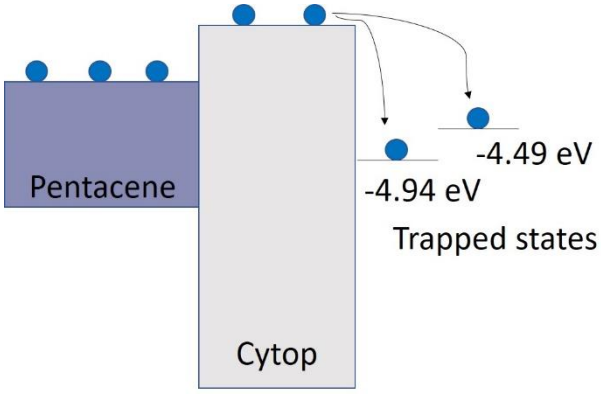

Fig. 5. *Trapping mechanism of electrons in the floating gate.*

3.3. Operation mechanism

Figure 5 shows the proposed mechanism operation of the memory OFET. When the programming voltage was applied, the electrons were injected from the S/D electrodes, travelling through the pentacene and Cytop layer and trapped at the $Li^+@C_{60}$ molecules at the surface of the floating gate. Each $Li^+@C_{60}$ molecule could trap up to 2 electrons at the LUMO level of -4.94 and -4.49 eV. When the programming duration increased, the number of active $Li^+@C_{60}$ molecules would increase, resulting in the increase of the trapped electron in the floating gate, causing the multi-level effect in the device [13]. When a reversed voltage was applied, the trapped electrons would de-trap since the high insulator of the SiO_2.

4. CONCLUSION

We demonstrated the operation mechanism of the multi-level memory OFET using $Li^+@C_{60}$ as a floating gate. The estimated number of trapped electrons per $Li^+@C_{60}$ molecule was calculated from the number of trapped electrons in the floating gate and the distribution of $Li^+@C_{60}$ molecules. It indicated the active $Li^+@C_{60}$ molecules are on the surface of the

floating gate. The analysis from the CV and UV-Vis measurement shows that each active $Li^+@C_{60}$ molecule could trap 2 electrons. From this research, the trapping mechanism of electrons in the floating gate of $Li^+@C_{60}$ has been clearly understood, which is the origin of the multi-level effect in our memory. We believe this result will help the evolution of the $Li^+@C_{60}$ research field, and reveals its potential for electric memory applications such as wearable devices, flying camera system, and Internet of Things applications

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